26.4 Wideband Image-Rejection Circuit for Low-IF Receivers

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Low-IF receivers are more robust to low-frequency disturbances such as dc offset and 1/f noise as compared to direct-conversion receivers. Thus, the performance requirements for the front-end circuits of low-IF systems is more relaxed. Consequently, the current consumption of the front-end circuits of such receivers is reduced and robustness against device variations is improved. However, a low-IF receiver has the fundamental issue of image-signal contamination due to circuit mismatch.

Figure 26.4.1 shows the relationship between frequency and power level of a desired signal and reference interferences defined in the GSM specification. The interference level is 9dB and 41dB higher than the desired-signal level for the adjacent interference (200kHz offset) and the bi-adjacent interference (400kHz offset), respectively. In a low-IF GSM receiver, if IF is chosen as 100kHz, the adjacent-channel frequency coincides with the image-signal frequency. In that case, the required image-rejection ratio (IRR) is about 32dB [1, 2], which is not too difficult to achieve with analog circuitry. However, in enhanced data for GSM evolution (EDGE) mode, when an 8PSK modulated signal is received, choosing a higher IF is preferable. Due to a larger image signal, a larger IRR is required. For example, when IF is chosen as 200kHz, the bi-adjacent channel frequency coincides with the image-signal frequency and at least 50dB IRR is required.

Generally, IRR is degraded by analog mismatch of I/Q mixers, analog filters, PGAs, and ADCs. To overcome this degradation, different schemes for correcting I/Q mismatch have been studied. However, previous works did not correct frequency-response mismatch [2] or required much time for correction [3] in order to improve IRR performance.

With the above circumstances in mind, a low-IF receiver with correction circuit is proposed. This receiver corrects not only I/Q gain and phase mismatch but also I/Q frequency-response mismatch. The proposed circuit can achieve an IRR of more than 50dB over the GMSK/8PSK signal BW. The correction system consists of a test-signal generator, an error-detection circuit, an I/Q mismatch correction circuit, and a correction circuit based on FIR filters for correcting frequency-response mismatch.

Figure 26.4.2 shows the low-IF receiver with this correction system. The test signal is fed to the I/Q mixers and divided into I and Q signals. The test signals pick up I/Q mismatch as they pass through I/Q mixers, filters, PGAs, and 14b ADCs. Additional mismatch is detected by an error-detection circuit that generates correction parameters a_0 and b_0. These parameters are for correcting phase and amplitude mismatch at test-signal frequency. For correcting frequency mismatch, a set of n discrete test-signal frequencies within the low-IF channel are chosen, and corresponding parameters $a_1,\ldots,a_n$ and $b_1,\ldots,b_n$ are generated. From these parameters for different frequencies, FIR filter coefficients are determined.

Figure 26.4.3 shows the details of the proposed error-detection circuit that has two convergence loops; one for phase mismatch and one for amplitude mismatch, and determines two parameters, a and b. The input signal is up-converted in the digital part of the receiver in order to reduce the delay time for convergence.

Figure 26.4.4 shows the test-signal generator. A 26MHz reference clock is fed into an inverter chain and generates higher harmonics. An RF differential amplifier amplifies the harmonic signals. The test-signal frequencies for the GSM850 and GSM900 bands are 884(=26×34)MHz and 936(=26×36)MHz, respectively. These signals are harmonics of the 26MHz reference frequency. Therefore, there is no image signal for low-IF receivers and hence, error-detecting accuracy is not degraded. As shown in Fig. 26.4.4, even with 34th and 36th harmonics, the corresponding IF signals can achieve an SNR of more than 65dB. Setting LO frequency at 100, 170, 230 and 300kHz offset from the above test-signal frequency provides a choice of test signal IF frequencies of 100, 170, 230, and 300kHz. Only one test-signal frequency can be used for each band, i.e., 884MHz for GSM850, and 936MHz for GSM900. The calculated LO phase mismatch within each band is no more than 0.026°, therefore, when LO phase mismatch is zero at the test-signal frequency, the correction data determined by using the above-mentioned test-signal frequencies can be applied to the other frequencies within the bands. The measurement results show that the corrected IRR degradation within each band is less than 1.35dB.

The overall system is implemented as a test IC (Figure 26.4.7), ADCs, DACs, and an FPGA circuit. The test IC consists of an LNA, I/Q mixers, PGAs, LPFs, a fractional-N synthesizer, and the test-signal generator.

Figure 26.4.5 shows how the correction parameter a settles over time. This parameter is monitored as an analog voltage signal through a DAC. It is clearly shown that the convergence of one correction parameter can be completed within 25µs.

Figure 26.4.6 shows the dependency of the measured IRR performance on frequency. Before the correction, IRR is around 30 to 40dB within the receiver band. Therefore, it does not meet the target specification. When correction is performed for one frequency, IRR is over 50dB at 200kHz (at which the correction is done). However, because of the mismatch in the LPF, IRR degrades as frequency diverges from 200kHz. On the other hand, when correction is performed for 4 frequencies, IRR is improved over a wide frequency range, thus meeting the target specification.

Figure 26.4.7 shows a micrograph of the test IC. Fabricated in a 0.25µm BiCMOS process, the chip occupies 10mm^2 and draws 80mA from a 2.8V supply. Other digital circuits are implemented on an FPGA with 46k gates, including all detection circuits, correction circuits and digital image-rejection mixer. These digital circuits will be integrated in an IC fabricated by a finer process without a serious impact on a total chip area.

In conclusion, the proposed correction scheme enables a low-IF receiver to use an IF higher than 100kHz and the IRR performance meets the GSM specification.

Acknowledgments:
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References:
[1] A.A. Abidi, "RF CMOS Comes of Age," *IEEE J. Solid-State Circuits*, vol. 39, no. 4, pp. 549-561, Apr., 2004.
[2] I. Elahi, K. Muhammad, and P.T. Balsara, "I/Q Mismatch Compensation in a 90nm Low-IF CMOS Receiver," *ISSCC Dig. Tech. Papers*, pp. 542-544, Feb., 2005.
[3] L. Yu and W.M. Snelgrove, "A Novel Adaptive Mismatch Cancellation System for Quadrature IF Radio Receivers," *IEEE Trans. Circuits Syst. II*, vol. 46, pp. 789-801, June 1999.

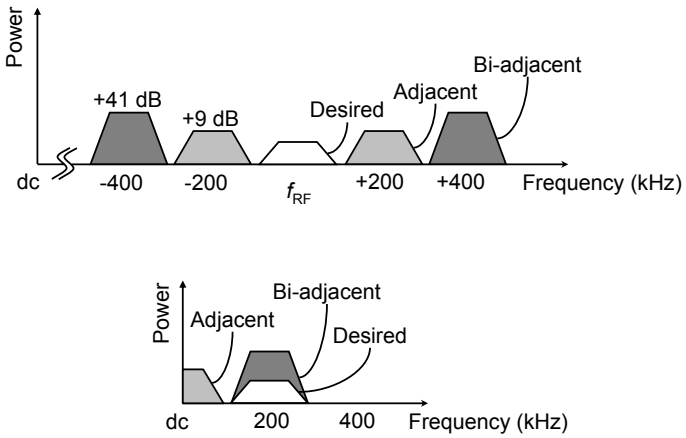

Figure 26.4.1: The desired signal and reference interferences.

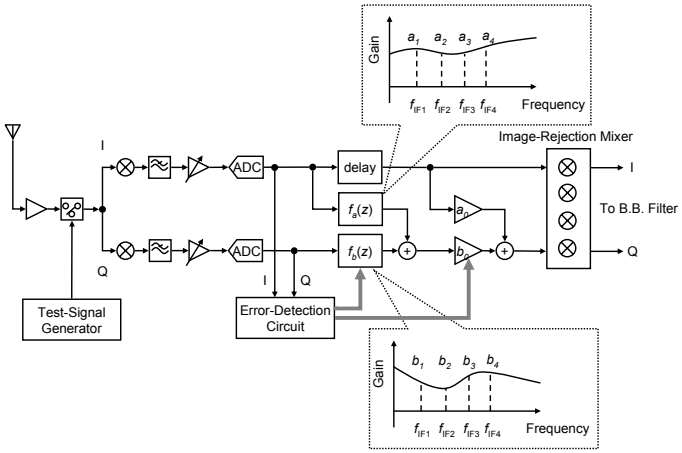

Figure 26.4.2: Proposed low-IF receiver architecture.

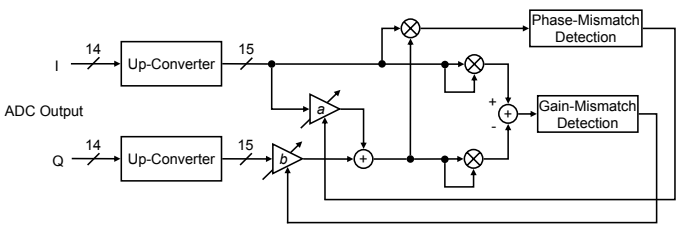

Figure 26.4.3: Error-detection circuit architecture.

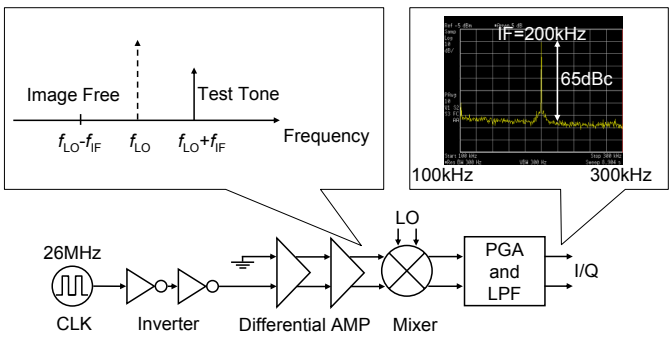

Figure 26.4.4: Test-signal generator.

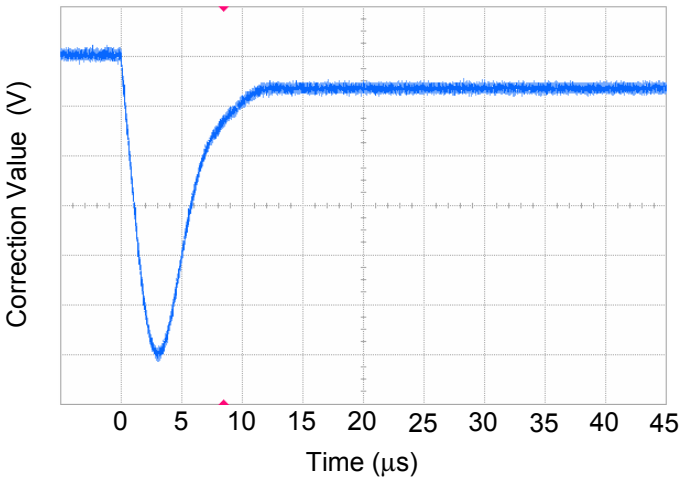

Figure 26.4.5: Measured convergence process.

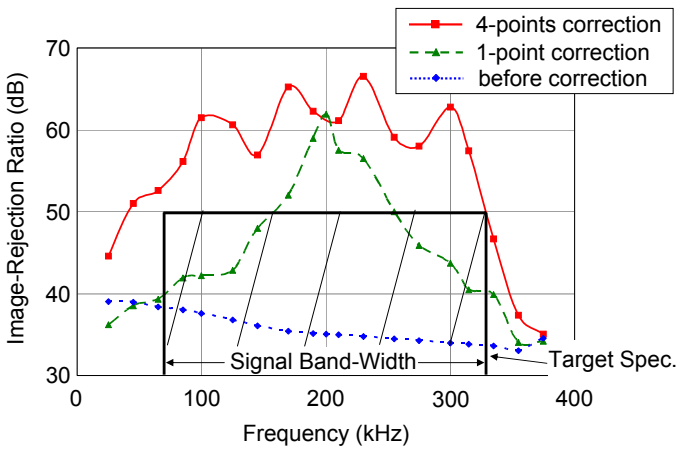

Figure 26.4.6: Measured image-rejection ratios.

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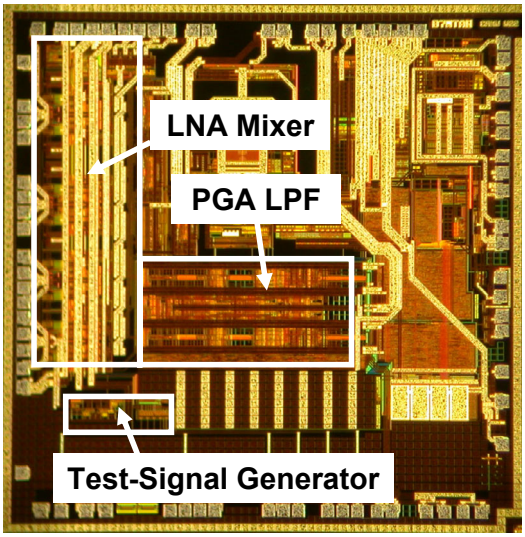

Figure 26.4.7: Chip micrograph.

